Abstracts

Effect of Device Layout on the Thermal Resistance of High-Power Thermally-Shunted Heterojunction Bipolar Transistors

R. Dettmer, T. Jenkins, J. Barrette, C. Bozada, G. DeSalvo, J. Ebel, J. Gillespie, C. Havasy, C. Ito, K. Nakano, C. Pettiford, T. Quach, J. Sewell, D. Via and R. Anholt. "Effect of Device Layout on the Thermal Resistance of High-Power Thermally-Shunted Heterojunction Bipolar Transistors." 1996 MTT-S International Microwave Symposium Digest 96.3 (1996 Vol. III [MWSYM]): 1607-1610.

The effect of device layout on thermal impedance of thermally-shunted HBTs was investigated. A direct comparison of thermally shunted devices and standard airbridge devices is made. Changes in thermal resistance of up to 67% were observed. While thermal resistance remains sensitive to emitter element placement in thermally shunted devices, variations in the location of thermal shunt landings had little effect. These results provide a basis for optimizing thermally-shunted devices.

❑ Return to main document.